PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Makoto KOBAYASHI et al. Group Art Unit: 3723

Application No.: 09/830,434 Examiner: H. Shakeri

Filed: April 26, 2001 Docket No.: 109352

For: POLISHING PAD AND POLISHING METHOD FOR SEMICONDUCTOR WAFER

AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

In reply to the Office Action mailed November 7, 2001, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claim 19 without prejudice to or disclaimer of the subject matter contained therein.

Please replace claims 15, 17, 18, 20-29 and 31 as follows:

15. (Amended) The polishing pad used for polishing a semiconductor wafer according to Claim 12, which comprises a base layer formed of nonwoven fabric and a porous surface layer.

17. (Amended) The polishing pad used for polishing a semiconductor wafer according to Claim 14, wherein a content of zinc compounds in the porous surface layer is 100ppm or less at the ratio of zinc weight relative to the weight of the porous surface layer.